AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

1. (currently amended) A manufacturing method of a semiconductor integrated circuit device comprising the steps of:

(a) depositing a positive type photoresist film on a semiconductor substrate;

(b) exposing a first mask pattern on said positive type photoresist film;

(c) exposing a second mask pattern on said positive type photoresist film so as to be superposed on said first mask pattern;

(d) performing development treatment relative to said positive type resist film after said steps (b) and (c) and thereby forming a photoresist pattern comprising a positive type photoresist pattern on said semiconductor substrate; and

(e) performing etching treatment relative to said semiconductor substrate by using said photoresist pattern as a mask and thereby transferring a transferred pattern on said semiconductor substrate,

wherein said first mask pattern is a pattern for transferring a gate pattern and has a pattern for transferring a line pattern; and

wherein said second mask pattern is a pattern for removing an unnecessary portion transferred on said positive type photoresist film at the

time of transfer using said first mask pattern and has a plurality of unit cells arranged regularly; and

wherein said second mask pattern has:

a plurality of main light transferring patterns for separating said line pattern;

a plurality of auxiliary light transferring patterns disposed such that a distance between each of said main light transferring patterns and each of said auxiliary light transferring patterns becomes the same in a periphery thereof, and formed at such a dimension as not to be transferred on said positive type photoresist film; and

a phase shifter disposed in any one of said main light transferring patterns and said auxiliary light transferring patterns and generating a phase difference in a transferring light.

2. (canceled).

3. (currently amended) The manufacturing method of a semiconductor integrated circuit device according to claim 21, wherein said gate pattern is a gate pattern in an SRAM memory cell.

4. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said auxiliary light transferring patterns arranged around each of said main light transferring patterns are disposed at respective corner

portions of a hexagon whose center coincides with a center of each of said main light transferring patterns.

5. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said auxiliary light transferring patterns arranged around each of said main light transferring patterns are disposed on an axis extending in a first direction passing through a center of each of said main light transferring patterns, and are not disposed on an axis extending in a second direction vertically intersecting relative to said first direction, and are symmetrically disposed relative to the axis extending in said second direction and being regarded as a center line.

6. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein a pitch between said main light transferring patterns adjacent to each other along an axis extending in a first direction is longer than a pitch between said main light transferring patterns adjacent to each other along an axis extending in a second direction vertically intersecting relative to said first direction passing through a center of each of said main light transferring patterns.

7. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 6,

wherein said pitch between said main light transferring patterns adjacent to each other along the axis extending in said second direction is a closest pitch, and

said closest pitch is within a range of 0.66/(λ/NA) to 0.9/(λ/NA) converted to a dimension of said semiconductor substrate, where a wavelength of exposure light used in said exposure treatment is λ and the numerical aperture of an optical lens of an exposure apparatus is NA.

8. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 1, further comprising a step of performing said exposure treatment by using a photomask forming said first and second mask patterns on the same mask substrate.

9. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 8,

wherein both exposure treatment using said first mask pattern and exposure treatment using said second mask pattern are used as scanning exposure treatment.

10. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein a condition of the exposure treatment using said first mask pattern is the same as a condition of the exposure treatment using said second mask pattern.

11. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said step (b) performs exposure treatment by using a first photomask on which said first mask pattern is formed, and

wherein said step (c) performs exposure treatment by using a second photomask which is different from said first photomask and on which said second mask pattern is formed.

12. (new) The manufacturing method of a semiconductor integrated circuit device according to claim 11,

wherein both exposure treatment using said first mask pattern and exposure treatment using said second mask pattern are used as scanning exposure treatment.